High K Oxides (Design Specifications and Challenge Mitigation)

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Since the introduction of integrated circuits (IC), much research has been focused on scaling feature sizes to ever smaller dimensions. This trend was described in 1965 by Dr. Gordon E. Moore where he predicted the number of transistors per chip to double every eighteen months.[1] Moore's Law, has served as a benchmark for the IC industry, ushering in the newest generation of components at the 45nm node.[2] Complementary Metal Oxide Semiconductor Field Effect Transistors (CMOS FET) have been the primary devices on an IC logic circuit. Utilizing a metal/oxide stack held at a controlled bias on a doped semiconductor substrate, the current between the source and drain can be manipulated, creating an on (I_{on}) or off (I_{off}) current.

Oxide layers serve as capacitors,[3] where capacitance, C, is

$$C = \frac{\varepsilon_o K A}{d}$$

and ε_o is permittivity of air, K is the dielectric constant, A is area, and d is oxide thickness. Oxide thickness of CMOS devices went below 2nm, only several atomic layers, thus reaching its physical and practical limitation.[2,4] Electron tunneling through these thin layers caused an unacceptably high leakage current and called for new materials to control this problem and allow for further scaling. [2]

Grown by thermal oxidation, SiO_2 has driven the semiconductor industry to unimaginable heights due in large part to its supreme interface with Si. High K oxides must be deposited; therefore a lower quality interface is expected. Atomic layer deposition[2,5-7] has shown to exhibit sub-monolayer control of film thickness,[8] however the presence of excess oxygen has led to oxidation of the Si subsurface increasing the effective oxide thickness (EOT) of the dielectric layer.[9]

$$EOT = \frac{K_{SiO2}}{K_{HighK}} d_{HighK} = \frac{3.9}{K_{HighK}} d_{HighK}$$

Moreover, grain boundaries promote diffusion of O and Si but cannot be easily avoided due to the low crystallization temperature of many high K oxides. Silicate and silicon dioxide interlayers will ultimately limit scalability.[10] Therefore, an abrupt high K oxide/Si interface is required to achieve the lowest EOT.

Choice of high K oxides has proven to be a difficult task, where parameters such as thermodynamic and kinetic stability, band offset, structural defects, etc, must be controlled.[2,4] Of paramount importance is the interface between silicon and the high K oxide. Controlling the Si/high K oxide interface will ensure minimal electronic defects serving as traps to charge carriers. Först, et al[4] performed a theoretical study of the interface between Si and $SrTiO_3$. Owing to the presence of dangling bonds[11] on a clean Si(001) surface, a ½ monolayer of Sr is first required to passivate the surface thereby removing any surface states in the band gap. Using this surface as a suitable building block for oxide layer formation, layers of SrO or $SrTiO_3$ can be deposited. An annealing cycle of 600K crystallizes the structure, forming an atomically abrupt interface. The

effects of oxidation were found to attack the empty Si coordination site. All coordination sites are occupied after addition of a full monolayer of O atoms.

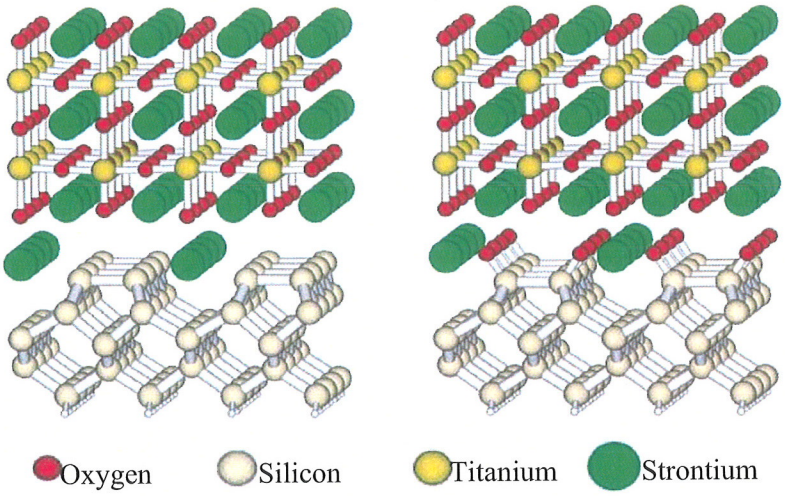

Figure 1: Si(001)/$SrTiO_3$ atomic structure, Sr passivated (left) and oxidized (right)

Park et al[7] have sputtered a thin (0.5nm) film of Hf on a HfO_2(5nm)/Si surface in attempt to suppress Si diffusion into the HfO_2 layer forming Hf-silicate. Owing to fewer nucleation sites under the top Hf metal layer, larger grain sizes were observed by high resolution transmission electron microscopy thereby reducing the grain boundary density. Similarly, Kobayashi et al[9] have deposited a thin (1nm) SiN layer followed by a 3nm HfO_2 layer to prevent diffusion of Hf and O and the subsequent interface reactions. EOT of the SiN-containing samples remain constant after a post-deposition anneal and show a lower leakage current density compared to that of the as-deposited SiN-containing samples.

References

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