Potentials and Pitfalls of Si Nanowire Electronics

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One dimensional nanoscale materials, such as nanowires (NW)[1] and carbon nanotubes (CNT)[2], are attractive building blocks for future nanoelectronic systems because of their ability to overcome the scaling limit of current top-down photolithography approach when combined with bottom-up self-assembly. Moreover, since those nanomaterials grown at high temperature can be assembled into active electronic devices over large area at room temperature, they are promising candidate in the field of "macroelectronics", defined as electronic systems fabricated over large/flexible substrate with low cost and acceptable performances.[3, 4] Here we review the progress made toward these goals with Si NWs and discussed their future challenges in real applications.

Si NWs are synthesized through vapor-liquid-solid synthesis or chemical vapor deposition (CVD) method from metal nanoclusters.[5] The diameter of Si NWs can be controlled by varying the diameter of catalyst[6] and the doping level can be controlled by adjusting the ratio between SiH_4 and B_2H_6/PH_3[7, 8]. The growth direction is determined by the surface energetics. Generally large NWs grow along <111> direction while the small NWs grow along <<110> direction (see Figure 1).[9] After synthesis, the Si NWs are collected from growth substrate and suspended in ethanol.

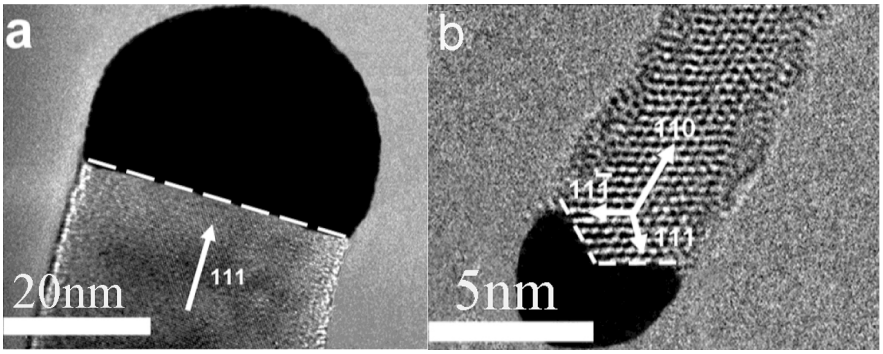

Figure 1: TEM image of the catalyst alloy/NW interface of a Si NW with a <111> growth axis (part a) and <110> growth axis (part b).

The fluidic flow-directed assembly approach can be used to align Si NWs on various substrates and organize Si NWs in to complex structures. In this method, Si NWs are aligned by passing a suspension of Si NW through microfluidic channel structure, typically formed between a poly(dimethylsiloxane) (PDMS) mold and a flat substarte.[10] The alignment of NWs within the channel flow can be understood within the framework of shear flow. Specifically, the channel flow near the substrate surface resembles a shear flow, and linear shear force aligns the NWs in the flow direction before they are immobilized on the substrate. The degree of alignment can be further increased when combined with complementary chemical interactions between chemically patterned substrate and Si NWs. In the field of macroelectronics, the ability to create metal features over large area in a cost-effective method at room temperature is also important. The nanoimprint lithography (NIL) provides a possible way to solve this problem (see Figure 2).[11]

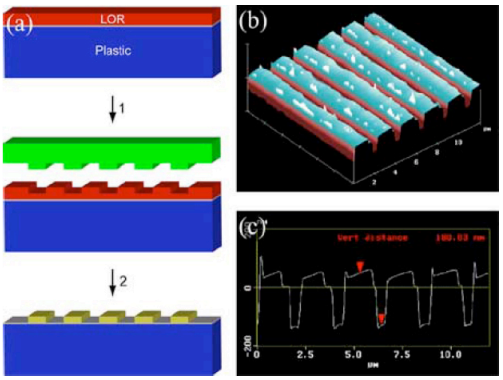

Fig. 2. a) Schematic of the NIL process on plastic. (b) and (c) AFM topographical and line-scan images of the imprinted features, respectively.

Various electronic devices, including p-n junctions[12], light emitting diodes[13], bipolar junction transistors[12] and junction field effect transistors (FET)[14] have been realized with cross NW structures. More advanced systems, such as logic gates, computation circuits[14] and decoders[15] are also constructed with Si NWs in the same manner (See Figure 3a). Thin film transistors (TFT) based on single Si NW are intensively studied with focus on improving device performances in term of mobility and on/off ratio.[8, 16] The large contact resistance is a major drawback of those devices and can be significantly reduced through thermal annealing and/or surface passivation. The device variations are much less compared with those built on other nanomaterials and demonstrate performance comparable with conventional devices. On the other hand, TFTs based on both single Si NW and Si NW arrays have been fabricated on glass/plastic substrate.[11, 17] The performances of those devices are better than those TFTs based on organic semiconductors and amorphous Si. Figure 3b shows the optical image of a three-stage ring oscillator on glass substrate based on Si NWs with cutoff frequency up to 10MHz.[18]

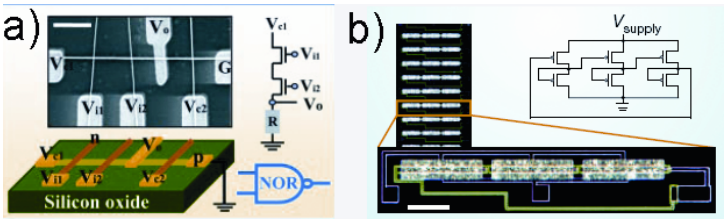

Figure 3: a) Schematic of logic NOR gate constructed from 1 by 3 crossed NW junction array. b) Optical images and circuit diagram of nanowire ring oscillators. Scale bar: 100μm.

However, for real applications in the next generation electronics Si NW still face lots and challenges. In the area of nanoelectronics, we still lack the ability to precisely control the doping levels and diameters of Si NWs. Moreover, the self assembly approach for pattering Si NW is only applicable for large Si NWs and the degree of integration is still limited. Although the size of Si NWs is in the *nano* regime, they haven't displayed any special properties compared with bulk Si, which is an obvious disadvantage compared with other nanomaterials such as CNTs. In the field of macroelectronics, the cost for Si NW is too high for this application and it is hard to compete with more mature techniques such as sequential laterally solidified polysilicon, which is compatible with existing fabrication process and have better performances.

References

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